How to Tune and Extract Higher Performance with MVAPICH2 Libraries?

An XSEDE ECSS webinar

by

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Drivers of Modern HPC Cluster Architectures

- Multi-core/many-core technologies
- Remote Direct Memory Access (RDMA)-enabled networking (InfiniBand and RoCE)
- Solid State Drives (SSDs), Non-Volatile Random-Access Memory (NVRAM), NVMe-SSD
- Accelerators (NVIDIA GPGPUs and Intel Xeon Phi)
Parallel Programming Models Overview

- Programming models provide abstract machine models
- Models can be mapped on different types of systems
  - e.g. Distributed Shared Memory (DSM), MPI within a node, etc.
- PGAS models and Hybrid MPI+PGAS models are gradually receiving importance
Overview of the MVAPICH2 Project

- High Performance open-source MPI Library for InfiniBand, 10-40Gig/iWARP, and RDMA over Converged Enhanced Ethernet (RoCE)
  - MVAPICH (MPI-1), MVAPICH2 (MPI-2.2 and MPI-3.0), Available since 2002
  - MVAPICH2-X (MPI + PGAS), Available since 2011
  - Support for GPGPUs (MVAPICH2-GDR) and MIC (MVAPICH2-MIC), Available since 2014
  - Support for Virtualization (MVAPICH2-Virt), Available since 2015
  - Support for Energy-Awareness (MVAPICH2-EA), Available since 2015
  - Used by more than 2,550 organizations in 79 countries
  - More than 363,000 (> 0.36 million) downloads from the OSU site directly
  - Empowering many TOP500 clusters (Nov ‘15 ranking)
    - 10th ranked 519,640-core cluster (Stampede) at TACC
    - 13th ranked 185,344-core cluster (Pleiades) at NASA
    - 25th ranked 76,032-core cluster (Tsubame 2.5) at Tokyo Institute of Technology and many others
  - Available with software stacks of many vendors and Linux Distros (RedHat and SuSE)
    - http://mvapich.cse.ohio-state.edu

- Empowering Top500 systems for over a decade
  - System-X from Virginia Tech (3rd in Nov 2003, 2,200 processors, 12.25 TFlops) ->
  - Stampede at TACC (10th in Nov’15, 519,640 cores, 5.168 Plops)
MVAPICH2 Architecture

High Performance Parallel Programming Models

| Message Passing Interface (MPI) | PGAS (UPC, OpenSHMEM, CAF, UPC++) | Hybrid --- MPI + X (MPI + PGAS + OpenMP/Cilk) |

High Performance and Scalable Communication Runtime

Diverse APIs and Mechanisms

| Point-to-point Primitives | Collectives Algorithms | Job Startup | Energy-Awareness | Remote Memory Access | I/O and File Systems | Fault Tolerance | Virtualization | Active Messages | Introspection & Analysis |

Support for Modern Networking Technology (InfiniBand, iWARP, RoCE, OmniPath)

<table>
<thead>
<tr>
<th>Transport Protocols</th>
<th>Modern Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC</td>
<td>UMR</td>
</tr>
<tr>
<td>XRC</td>
<td>ODP*</td>
</tr>
<tr>
<td>UD</td>
<td>SR-IOV</td>
</tr>
<tr>
<td>DC</td>
<td>Multi Rail</td>
</tr>
</tbody>
</table>

Support for Modern Multi-/Many-core Architectures (Intel-Xeon, OpenPower, Xeon-Phi (MIC, KNL*), NVIDIA GPGPU)

<table>
<thead>
<tr>
<th>Transport Mechanisms</th>
<th>Modern Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shared Memory</td>
<td>MCDRAM*</td>
</tr>
<tr>
<td>CMA</td>
<td>NVLink*</td>
</tr>
<tr>
<td>IVSHMEM</td>
<td>CAPI*</td>
</tr>
</tbody>
</table>

* Upcoming
MVAPICH/MVAPICH2 Release Timeline and Downloads

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XSEDE-ECSS

Number of Downloads vs Timeline

- MV 0.9.4
- MV2 0.9.0
- MV2 0.9.8
- MV1 0.0
- MV2 1.0
- MV2 1.0.3
- MV1 1.1
- MV2 1.4
- MV2 1.5
- MV2 1.6
- MV2 1.7
- MV2 1.8
- MV2 1.9
- MV2-GDR 2.0b
- MV2-MIC 2.0
- MV2 2.1
- MV2-GDR 2.2b
- MV2-Virt 2.1r2
- MV2-GDR 2.2rc1
- MV2-Virt 2.2rc1
- MV2 2.2rc1
- MV2 2.2rc1

Timeline:
- Sep-04
- Dec-04
- Mar-05
- Jun-05
- Sep-05
- Dec-05
- Mar-06
- Jun-06
- Sep-06
- Dec-06
- Mar-07
- Jun-07
- Sep-07
- Dec-07
- Mar-08
- Jun-08
- Sep-08
- Dec-08
- Mar-09
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- Sep-13
- Dec-13
- Mar-14
- Jun-14
- Sep-14
- Dec-14
- Mar-15
- Jun-15
- Sep-15
- Dec-15
# MVAPICH2 Software Family

<table>
<thead>
<tr>
<th>Requirements</th>
<th>MVAPICH2 Library to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPI with IB, iWARP and RoCE</td>
<td>MVAPICH2</td>
</tr>
<tr>
<td>Advanced MPI, OSU INAM, PGAS and MPI+PGAS with IB and RoCE</td>
<td>MVAPICH2-X</td>
</tr>
<tr>
<td>MPI with IB &amp; GPU</td>
<td>MVAPICH2-GDR</td>
</tr>
<tr>
<td>MPI with IB &amp; MIC</td>
<td>MVAPICH2-MIC</td>
</tr>
<tr>
<td>HPC Cloud with MPI &amp; IB</td>
<td>MVAPICH2-Virt</td>
</tr>
<tr>
<td>Energy-aware MPI with IB, iWARP and RoCE</td>
<td>MVAPICH2-EA</td>
</tr>
</tbody>
</table>
Strong Procedure for Design, Development and Release

- Research is done for exploring new designs
- Designs are first presented to conference/journal publications
- Best performing designs are incorporated into the codebase
- Rigorous Q&A procedure before making a release
  - Exhaustive unit testing
  - Various test procedures on diverse range of platforms and interconnects
  - Performance tuning
  - Applications-based evaluation
  - Evaluation on large-scale systems
- Even alpha and beta versions go through the above testing
Presentation Overview

- Runtime Optimization and Tuning Flexibility in
  - MVAPICH2 / MVAPICH2-X
    - Job start-up
    - Point-to-point Inter-node Protocol
    - Transport Type Selection
    - Point-to-point Intra-node Protocol and Scheme
    - Collectives
  - MVAPICH2-GDR
    - Coda-aware MPI
    - GPUDirect RDMA (GDR) Features
    - Tuning and Optimizations

- Application Best Practices
  - Amber, MiniAMR, SMG2000, Neuron, HPCCG, LULESH, MILC and HoomDBlue

- Conclusions and Final Q&A
### MVAPICH2 Interfaces (Latest Release 2.2rc1)

<table>
<thead>
<tr>
<th>MPI Application</th>
<th>Process Manager</th>
</tr>
</thead>
<tbody>
<tr>
<td>MVAPICH2</td>
<td></td>
</tr>
<tr>
<td>CH3 (OSU enhanced)</td>
<td>Nemesis</td>
</tr>
<tr>
<td>OFA-IB</td>
<td>mpirun_rsh</td>
</tr>
<tr>
<td>OFA-iWARP</td>
<td>mpirun, mpiexec, mpiexec.hydra</td>
</tr>
<tr>
<td>OFA-RoCE (v1/v2)</td>
<td></td>
</tr>
<tr>
<td>TrueScale (PSM)</td>
<td></td>
</tr>
<tr>
<td>Omni-Path (PSM2)</td>
<td></td>
</tr>
<tr>
<td>Shared-Memory</td>
<td></td>
</tr>
<tr>
<td>TCP/IP</td>
<td></td>
</tr>
<tr>
<td>OFA-IB (OSU enhanced)</td>
<td></td>
</tr>
<tr>
<td>TCP/IP</td>
<td></td>
</tr>
<tr>
<td>Shared-Memory</td>
<td></td>
</tr>
</tbody>
</table>

**All Different PCI interfaces**

**Major Computing Platforms:** IA-32, EM64T, OpenPower, Nehalem, Westmere, Sandybridge, Ivybridge, Haswell, Opteron, Magny, ..
Features of MVAPICH2 2.2rc1

• Released on 03/30/2016

• Major Features and Enhancements
  – Based on MPICH-3.1.4
  – Support for OpenPower architecture
    • Optimized inter-node and intra-node communication
  – Support for Intel Omni-Path architecture
    • Thanks to Intel for contributing the patch
    • Introduction of a new PSM2 channel for Omni-Path
  – Support for RoCEv2
  – Architecture detection for PSC Bridges system with Omni-Path
  – Enhanced startup performance and reduced memory footprint for storing InfiniBand end-point information with SLURM
    • Support for shared memory based PMI operations
    • Availability of an updated patch from the MVAPICH project website with this support for SLURM installations
  – Optimized pt-to-pt and collective tuning for Chameleon InfiniBand systems at TACC/UoC
  – Enable affinity by default for TrueScale(PSM) and Omni-Path(PSM2) channels
  – Enhanced tuning for shared-memory based MPI_Bcast
  – Enhanced debugging support and error messages
  – Update to hwloc version 1.11.2
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Towards High Performance and Scalable Startup at Exascale

- Near-constant MPI and OpenSHMEM initialization time at any process count
- 10x and 30x improvement in startup time of MPI and OpenSHMEM respectively at 16,384 processes
- Memory consumption reduced for remote endpoint information by $O(\text{processes per node})$
- 1GB Memory saved per node with 1M processes and 16 processes per node

**On-demand Connection Management for OpenSHMEM and OpenSHMEM+MPI.** S. Chakraborty, H. Subramoni, J. Perkins, A. A. Awan, and D K Panda, 20th International Workshop on High-level Parallel Programming Models and Supportive Environments (HIPS ’15)

**PMI Extensions for Scalable MPI Startup.** S. Chakraborty, H. Subramoni, A. Moody, J. Perkins, M. Arnold, and D K Panda, Proceedings of the 21st European MPI Users’ Group Meeting (EuroMPI/Asia ’14)


**SHMEMPMI – Shared Memory based PMI for Improved Performance and Scalability.** S. Chakraborty, H. Subramoni, J. Perkins, and D K Panda, 16th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid ’16), Accepted for Publication
Job-Launchers supported by MVAPICH2

Core Launchers

- mpirun_rsh
  - Default and preferred launcher for all interfaces
  - Supports scalable hierarchical job-startup mechanism

- mpiexec.hydra
  Developed at ANL by the MPICH team

Wrappers and interfaces

- mpiexec
  To support interfaces prescribed by the MPI standard

- mpiexec.mpirun_rsh
  Hydra-like interface to mpirun_rsh

SLURM
Compatibility with external resource managers

TORQUE
Tuning Job-Lauch with mpirun_rsh

- **MV2_MT_DEGREE**
  - degree of the hierarchical tree used by mpirun_rsh

- **MV2_FASTSSH_THRESHOLD**
  - #nodes beyond which hierarchical-ssh scheme is used

- **MV2_NPROCS_THRESHOLD**
  - #nodes beyond which file-based communication is used for hierarchical-ssh during start up

- **MV2_HOMOGENEOUS_CLUSTER**
  - Setting it optimizes startup for homogeneous clusters

- **MV2_ON_DEMAND_UD_INFO_EXCHANGE**
  - To optimize start-up by exchanging UD connection info on-demand
Performance of MPI_Init and Hello World at Large Scale on TACC Stampede

- Near-constant MPI_Init at any scale
- PMI Exchange costs overlapped with application computation
- MPI_Init is 59 times faster at 8,192 processes (512 nodes)
- Hello World (MPI_Init + MPI_Finalize) takes 5.7 times less time at 8,192 processes
- New designs show good scaling with 16K processes and above
- Available since MVAPICH2-2.1 and as patch for SLURM

TACC Stampede - Connect-IB (54 Gbps): 2.6 GHz Quad Octa-core (SandyBridge) Intel PCI Gen3 with Mellanox IB FDR

Process Management Interface over Shared Memory (SHMEMPMEI)

- SHMEMPMEI allows MPI processes to directly read remote endpoint (EP) information from the process manager through shared memory segments.
- Only a single copy per node - $O(\text{processes per node})$ reduction in memory usage.
- Estimated savings of 1GB per node with 1 million processes and 16 processes per node.
- Up to 1,000 times faster PMI Gets compared to default design.
- Available for MVAPICH2 2.2rc1 and SLURM-15.08.8.

Presentation Overview

- **Runtime Optimization and Tuning Flexibility in**
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- **Application Best Practices**
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- **Conclusions and Final Q&A**
Inter-node Point-to-Point Tuning: Eager Thresholds

- Switching Eager to Rendezvous transfer
  - Default: Architecture dependent on common platforms, in order to achieve both best performance and memory footprint
  - Threshold can be modified by users to get smooth performance across message sizes
    - mpirun_rsh –np 2 –f hostfile MV2_IBA_EAGER_THRESHOLD=32K a.out
    - Memory footprint can increase along with eager threshold
Inter-node Point-to-Point Tuning: Number of Buffers and RNDV Protocols

- RDMA Fast Path has advantages for smaller message range (default is on)
  - Disable: `mpirun_rsh -np 2 -f hostfile MV2_USE_RDMA_FASTPATH=0 a.out`
- Adjust the number of RDMA Fast Path buffers (benchmark window size = 64):
  - `mpirun_rsh -np 2 -f hostfile MV2_NUM_RDMA_BUFFER=64 a.out`
- Switch between Rendezvous protocols depending on applications:
  - `mpirun_rsh -np 2 -f hostfile MV2_RNDV_PROTOCOL=RGET a.out` (Default: RPUT)
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Using Shared Receive Queues with MVAPICH2

- SRQ reduces the memory used by $\frac{1}{6}$ at 64,000 processes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Significance</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_SRQ</td>
<td>• Enable / Disable use of SRQ in MVAPICH2</td>
<td>Enabled</td>
<td>• Always Enable</td>
</tr>
<tr>
<td>MV2_SRQ_MAX_SIZE</td>
<td>• Limits the maximum size of the SRQ</td>
<td>4096</td>
<td>• Increase to 8192 for large scale runs</td>
</tr>
<tr>
<td></td>
<td>• Places upper bound on amount of memory used for SRQ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MV2_SRQ_SIZE</td>
<td>• Number of buffers posted to the SRQ</td>
<td>256</td>
<td>• Upper Bound: MV2_SRQ_MAX_SIZE</td>
</tr>
<tr>
<td></td>
<td>• Automatically doubled by MVAPICH2 on receiving SRQ LIMIT EVENT from IB HCA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Refer to Shared Receive Queue (SRQ) Tuning section of MVAPICH2 user guide for more information

- [http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-1020008.5](http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-1020008.5)
Using eXtended Reliable Connection (XRC) in MVAPICH2

- Memory usage for 32K processes with 8-cores per node can be 54 MB/process (for connections)
- NAMD performance improves when there is frequent communication to many peers
- Enabled by setting `MV2_USE_XRC` to 1 (Default: Disabled)
- Requires OFED version > 1.3
  - Unsupported in earlier versions (< 1.3), OFED-3.x and MLNX_OFED-2.0
  - MVAPICH2 build process will automatically disable XRC if unsupported by OFED
- Automatically enables SRQ and ON-DEMAND connection establishment
- Refer to eXtended Reliable Connection (XRC) section of MVAPICH2 user guide for more information
- [http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-1030008.6](http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-1030008.6)
Using UD Transport with MVAPICH2

Memory Footprint of MVAPICH2

<table>
<thead>
<tr>
<th>Number of Processes</th>
<th>Conn.</th>
<th>Buffers</th>
<th>Struct</th>
<th>Total</th>
<th>Buffers</th>
<th>Struct</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>512</td>
<td>22.9</td>
<td>24</td>
<td>0.3</td>
<td>47.2</td>
<td>24</td>
<td>0.2</td>
<td>24.2</td>
</tr>
<tr>
<td>1024</td>
<td>29.5</td>
<td>24</td>
<td>0.6</td>
<td>54.1</td>
<td>24</td>
<td>0.4</td>
<td>24.4</td>
</tr>
<tr>
<td>2048</td>
<td>42.4</td>
<td>24</td>
<td>1.2</td>
<td>67.6</td>
<td>24</td>
<td>0.9</td>
<td>24.9</td>
</tr>
</tbody>
</table>

• Can use UD transport by configuring MVAPICH2 with the `--enable-hybrid` flag
  – Reduces QP cache trashing and memory footprint at large scale

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Significance</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_ONLY_UD</td>
<td>• Enable only UD transport in hybrid configuration mode</td>
<td>Disabled</td>
<td>• RC/XRC not used</td>
</tr>
<tr>
<td>MV2_USE_UD_ZCOPY</td>
<td>• Enables zero-copy transfers for large messages on UD</td>
<td>Enabled</td>
<td>• Always Enable when UD enabled</td>
</tr>
<tr>
<td>MV2_UD_RETRY_TIMEOUT</td>
<td>• Time (in usec) after which an unacknowledged message will be retried</td>
<td>500000</td>
<td>• Increase appropriately on large / congested systems</td>
</tr>
<tr>
<td>MV2_UD_RETRY_COUNT</td>
<td>• Number of retries before job is aborted</td>
<td>1000</td>
<td>• Increase appropriately on large / congested systems</td>
</tr>
</tbody>
</table>

Performance with SMG2000

- Refer to Running with scalable UD transport section of MVAPICH2 user guide for more information
- [http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-640006.10](http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-640006.10)
Hybrid (UD/RC/XRC) Mode in MVAPICH2

- Both UD and RC/XRC have benefits
  - Hybrid for the best of both
- Enabled by configuring MVAPICH2 with the \texttt{--enable-hybrid}
- Available since MVAPICH2 1.7 as integrated interface

![Performance with HPCC Random Ring](image)

<table>
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<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_UD_HYBRID</td>
<td>• Enable / Disable use of UD transport in Hybrid mode</td>
<td>Enabled</td>
<td>• Always Enable</td>
</tr>
<tr>
<td>MV2_HYBRID_ENABLE_THRESHOLD_SIZE</td>
<td>• Job size in number of processes beyond which hybrid mode will be enabled</td>
<td>1024</td>
<td>• Uses RC/XRC connection until job size &lt; threshold</td>
</tr>
<tr>
<td>MV2_HYBRID_MAX_RC_CONN</td>
<td>• Maximum number of RC or XRC connections created per process</td>
<td>64</td>
<td>• Prevents HCA QP cache thrashing</td>
</tr>
<tr>
<td></td>
<td>• Limits the amount of connection memory</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Refer to Running with Hybrid UD-RC/XRC section of MVAPICH2 user guide for more information
- [http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-650006.11](http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-650006.11)
Minimizing Memory Footprint by Direct Connect (DC) Transport

- Constant connection cost (*One QP for any peer*)
- Full Feature Set (RDMA, Atomics etc)
- Separate objects for send (DC Initiator) and receive (DC Target)
  - DC Target identified by “DCT Number”
  - Messages routed with (DCT Number, LID)
  - Requires same “DC Key” to enable communication
- Available since MVAPICH2-X 2.2a

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- Application Best Practices
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- Conclusions and Final Q&A
Intra-node Communication Support in MVAPICH2

- **Shared-Memory based two-copy intra-node communication**
  - Copy from the sender’s user buffer to the shared buffer
  - Copy from the shared buffer to the receiver’s user buffer

- **LiMIC2 on modern multi-core platforms**
  - Kernel-level module for achieving single copy intra-node communication
  - LiMIC2 is used for rendezvous protocol message size
  - LiMIC2 module is required

- **CMA (Cross Memory Attach) support**
  - Single copy intra-node communication through Linux syscalls
  - Available from Linux kernel 3.2
MVAPICH2 Two-Sided Intra-Node Tuning:
Shared memory and Kernel-based Zero-copy Support (LiMIC and CMA)

- **LiMIC2:**
  - configure the library with ‘--with-limic2’
  - mpirun_rsh –np 2 –f hostfile a.out (To disable: MV2_SMP_USE_LIMIC2=0)
- **CMA:**
  - configure the library with ‘--with-cma’
  - mpirun_rsh –np 2 –f hostfile a.out (To disable: MV2_SMP_USE_CMA=0)
- When both ‘--with-limic2’ and ‘--with-cma’ are included at the same time, LiMIC2 is chosen by default
- When neither ‘--with-limic2’ or ‘--with-cma’ is used during in configuration, shared-memory based design is chosen
MVAPICH2 Two-Sided Intra-Node Tuning: Shared-Memory based Runtime Parameters

- Adjust eager threshold and eager buffer size:
  - `mpirun_rsh -np 2 -f hostfile MV2_SMP_EAGERSIZE=16K MV2_SMPI_LENGTH_QUEUE=64 a.out`
  - Will affect the performance of small messages and memory footprint
- Adjust number of buffers and buffer size for shared-memory based Rendezvous protocol:
  - `mpirun_rsh -np 2 -f hostfile MV2_SMP_SEND_BUFFER=32 MV2_SMP_SEND_BUFF_SIZE=8192 a.out`
  - Will affect the performance of large messages and memory footprint
Impact of Architecture-Specific Tuning

- Architecture-specific tuning is executed for new architectures and new designs introduced into MVAPICH2
- MV2_SMP_EAGERSIZE and MV2_SMP_SEND_BUFF_SIZE are updated from Default to Tuned
Presentation Overview

- Runtime Optimization and Tuning Flexibility in
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    - Tuning and Optimizations

- Application Best Practices
  - Amber, MiniAMR, SMG2000, Neuron, HPCCG, LULESH, MILC and HoomDBlue

- Conclusions and Final Q&A
Collective Communication in MVAPICH2

Run-time flags:
All shared-memory based collectives: MV2_USE_SHMEM_COLL (Default: ON)
Hardware Mcast-based collectives: MV2_USE_MCAST (Default: OFF)
Hardware Multicast-aware MPI_Bcast on TACC Stampede

- MCAST-based designs improve latency of MPI_Bcast by up to 85%
- Use MV2_USE_MCAST = 1 to enable MCAST-based designs
Enabling MCAST-based designs for MPI_Scatter improves small message up to **75%**

- Use `MV2_USE_MCAST = 1` to enable MCAST-based designs
Enabling Hardware Multicast-aware

- Multicast is applicable to
  - MPI_Bcast
  - MPI_Scatter
  - MPI_Allreduce

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Default Nature</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_MCAST = 1</td>
<td>Enables hardware Multicast features</td>
<td>Disabled</td>
</tr>
<tr>
<td>--enable-mcast</td>
<td>Configure flag to enable</td>
<td>Enabled</td>
</tr>
</tbody>
</table>

- Refer to Running Collectives with Hardware based Multicast support section of MVAPICH2 user guide for more information
- [http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-620006.8](http://mvapich.cse.ohio-state.edu/static/media/mvapich/mvapich2-2.2rc1-userguide.html#x1-620006.8)
Shared-memory Aware Collectives

- MVAPICH2 Reduce/Allreduce with 4K cores on TACC Ranger (AMD Barcelona, SDR IB)
- MVAPICH2 Barrier with 1K Intel Westmere cores, QDR IB

MV2_USE_SHMEM_REDUCE=0/1

MV2_USE_SHMEM_ALLREDUCE=0/1

MV2_USE_SHMEM_BARRIER=0/1
Non-Blocking Collectives in MVAPICH2

- MVAPICH2 supports for MPI-3 Non-Blocking Collective communication and Neighborhood collective communication primitives
  - MVAPICH2 1.9 to MVAPICH2 2.2
- MPI-3 collectives in MVAPICH2 can use either the Gen2 or the nemesis interfaces, over InfiniBand
- MVAPICH2 implements non-blocking collectives either in a multi-core-aware hierarchical manner, or via a basic flat approach
- Application developers can use MPI-3 collectives to achieve computation/communication overlap
Modified P3DFFT with Offload-Alltoall does up to 17% better than default version (128 Processes)

Modified Pre-Conjugate Gradient Solver with Offload-Allreduce does up to 21.8% better than default version

Modified HPL with Offload-Bcast does up to 4.5% better than default version (512 Processes)

K. Kandalla, et. al. High-Performance and Scalable Non-Blocking All-to-All with Collective Offload on InfiniBand Clusters: A Study with Parallel 3D FFT

K. Kandalla, et al, Designing Non-blocking Broadcast with Collective Offload on InfiniBand Clusters: A Case Study with HPL, HotI 2011

K. Kandalla, et. al., Designing Non-blocking Allreduce with Collective Offload on InfiniBand Clusters: A Case Study with Conjugate Gradient Solvers, IPDPS ’12

Presentation Overview

• **Runtime Optimization and Tuning Flexibility in**
  - MVAPICH2 / MVAPICH2-X
    • Job start-up
    • Point-to-point Inter-node Protocol
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• **Application Best Practices**
  - Amber, MiniAMR, SMG2000, Neuron, HPCCG, LULESH, MILC and HoomDBlue

• **Conclusions and Final Q&A**
GPU-Aware MPI Library: MVAPICH2-GPU

- Standard MPI interfaces used for unified data movement
- Takes advantage of Unified Virtual Addressing (>= CUDA 4.0)
- Overlaps data movement from GPU with RDMA transfers

**At Sender:**

```c
MPI_Send(s_devbuf, size, ...);
```

**At Receiver:**

```c
MPI_Recv(r_devbuf, size, ...);
```

*High Performance and High Productivity*
GPU-Direct RDMA (GDR) with CUDA

- OFED with support for GPUDirect RDMA is developed by NVIDIA and Mellanox
- OSU has a design of MVAPICH2 using GPUDirect RDMA
  - Hybrid design using GPU-Direct RDMA
    - GPUDirect RDMA and Host-based pipelining
    - Alleviates P2P bandwidth bottlenecks on SandyBridge and IvyBridge
  - Support for communication using multi-rail
  - Support for Mellanox Connect-IB and ConnectX VPI adapters
  - Support for RoCE with Mellanox ConnectX VPI adapters

SNB E5-2670 / IVB E5-2680V2

SNB E5-2670
P2P write: 5.2 GB/s
P2P read: < 1.0 GB/s

IVB E5-2680V2
P2P write: 6.4 GB/s
P2P read: 3.5 GB/s
CUDA-Aware MPI: MVAPICH2-GDR 1.8-2.2 Releases

- Support for MPI communication from NVIDIA GPU device memory
- High performance RDMA-based inter-node point-to-point communication (GPU-GPU, GPU-Host and Host-GPU)
- High performance intra-node point-to-point communication for multi-GPU adapters/node (GPU-GPU, GPU-Host and Host-GPU)
- Taking advantage of CUDA IPC (available since CUDA 4.1) in intra-node communication for multiple GPU adapters/node
- Optimized and tuned collectives for GPU device buffers
- MPI datatype support for point-to-point and collective communication from GPU device buffers
Performance of MVAPICH2-GPU with GPU-Direct RDMA (GDR)

GPU-GPU internode latency

- MV2-GDR2.2b
- MV2-GDR2.0b
- MV2 w/o GDR

Latency (us)

Message Size (bytes)

GPU-GPU Internode Bandwidth

- MV2-GDR2.2b
- MV2-GDR2.0b
- MV2 w/o GDR

Bandwidth (MB/s)

Message Size (bytes)

GPU-GPU Internode Bi-Bandwidth

- MV2-GDR2.2b
- MV2-GDR2.0b
- MV2 w/o GDR

Bi-Bandwidth (MB/s)

Message Size (bytes)

MVAPICH2-GDR-2.2b
Intel Ivy Bridge (E5-2680 v2) node - 20 cores
NVIDIA Tesla K40c GPU
Mellanox Connect-IB Dual-FDR HCA
CUDA 7
Mellanox OFED 2.4 with GPU-Direct-RDMA
Application-Level Evaluation (HOOMD-blue)

- Platform: Wilkes (Intel Ivy Bridge + NVIDIA Tesla K20c + Mellanox Connect-IB)
- HoomdBlue Version 1.0.5
  - GDRCOPY enabled: MV2_USE_CUDA=1 MV2_IBA_HCA=mlx5_0 MV2_IBA_EAGER_THRESHOLD=32768 MV2_VBUF_TOTAL_SIZE=32768 MV2_USE_GPUDIRECT_LOOPBACK_LIMIT=32768 MV2_USE_GPUDIRECT_GDRCOPY=1 MV2_USE_GPUDIRECT_GDRCOPY_LIMIT=16384

---

**64K Particles**

<table>
<thead>
<tr>
<th>Number of Processes</th>
<th>Average Time Steps per second (TPS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>MV2: 1500, MV2+GDR: 3000</td>
</tr>
<tr>
<td>8</td>
<td>MV2: 1250, MV2+GDR: 2500</td>
</tr>
<tr>
<td>16</td>
<td>MV2: 1000, MV2+GDR: 2000</td>
</tr>
<tr>
<td>32</td>
<td>MV2: 750,  MV2+GDR: 1500</td>
</tr>
</tbody>
</table>

**256K Particles**

<table>
<thead>
<tr>
<th>Number of Processes</th>
<th>Average Time Steps per second (TPS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>MV2: 1000, MV2+GDR: 2000</td>
</tr>
<tr>
<td>8</td>
<td>MV2: 750,  MV2+GDR: 1500</td>
</tr>
<tr>
<td>16</td>
<td>MV2: 500,   MV2+GDR: 1000</td>
</tr>
<tr>
<td>32</td>
<td>MV2: 250,   MV2+GDR: 500</td>
</tr>
</tbody>
</table>

- 2X speedup compared to baseline MV2.

Platform: Wilkes: Intel Ivy Bridge
NVIDIA Tesla K20c + Mellanox Connect-IB
Available since MVAPICH2-GDR 2.2a
Using MVAPICH2-GDR Version

• MVAPICH2-GDR 2.2b with GDR support can be downloaded from https://mvapich.cse.ohio-state.edu/download/#mv2gdr/

• System software requirements
  • Mellanox OFED 2.1 or later
  • NVIDIA Driver 331.20 or later
  • NVIDIA CUDA Toolkit 6.0 or later
  • Plugin for GPUDirect RDMA
    – Strongly Recommended: use the new GDRCOPY module from NVIDIA
      • https://github.com/NVIDIA/gdrcopy
  
• Has optimized designs for point-to-point communication using GDR
• Can also be run without GDR (have better performance benefits compared to MVAPICH2)
• Contact MVAPICH help list with any questions related to the package
  mvapich-help@cse.ohio-state.edu
Presentation Overview

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• Conclusions and Final Q&A
### Pipelined Data Movement in MVAPICH2-GDR: Tuning

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Significance</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_CUDA</td>
<td>• Enable / Disable GPU designs</td>
<td>0       (Disabled)</td>
<td>• Disabled to avoid pointer checking overheads for host communication</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Always enable to support MPI communication from GPU Memory</td>
</tr>
<tr>
<td>MV2_CUDA_BLOCK_SIZE</td>
<td>• Controls the pipeline blocksize</td>
<td>256 KByte</td>
<td>• Tune for your system and application</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Varies based on</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- CPU Platform, IB HCA and GPU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- CUDA driver version</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Communication pattern (latency/bandwidth)</td>
</tr>
</tbody>
</table>

- Refer to Tuning and Usage Parameters section of MVAPICH2-GDR user guide for more information
- [http://mvapich.cse.ohio-state.edu/userguide/gdr/#_tuning_and_usage_parameters](http://mvapich.cse.ohio-state.edu/userguide/gdr/#_tuning_and_usage_parameters)
# Tuning GPUDirect RDMA (GDR) Designs in MVAPICH2-GDR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Significance</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_USE_GPUDIRECT</td>
<td>• Enable / Disable GDR-based designs</td>
<td>1</td>
<td>• Always enable</td>
</tr>
</tbody>
</table>
| MV2_GPUDIRECT_LIMIT           | • Controls messages size until which GPUDirect RDMA is used | 8 KByte  | • Tune for your system
• GPU type, host architecture and CUDA version: impact pipelining overheads and P2P bandwidth bottlenecks |

- Refer to Tuning and Usage Parameters section of MVAPICH2-GDR user guide for more information
- [http://mvapich.cse.ohio-state.edu/userguide/gdr/#_tuning_and_usage_parameters](http://mvapich.cse.ohio-state.edu/userguide/gdr/#_tuning_and_usage_parameters)
### Runtime Parameters

- Works between GPUs within the same socket or IOH

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Significance</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MV2_CUDA_IPC</td>
<td>• Enable / Disable CUDA IPC-based designs</td>
<td>1 (Enabled)</td>
<td>• Always leave set to 1</td>
</tr>
<tr>
<td>MV2_CUDA_SMP_IPC</td>
<td>• Enable / Disable CUDA IPC fastpath design for short messages</td>
<td>0 (Disabled)</td>
<td>• Benefits Device-to-Device transfers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Hurts Device-to-Host/Host-to-Device transfers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Always set to 1 if application involves only Device-to-Device transfers</td>
</tr>
</tbody>
</table>

**Intranode osu_latency small**

![Graph showing latency against message size](chart)

**Legend:**
- **SHARED-MEM**
- **IPC**
- **SMP-IPC**
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- Application Best Practices
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- Conclusions and Final Q&A
Applications-Level Tuning: Compilation of Best Practices

• MPI runtime has many parameters
• Tuning a set of parameters can help you to extract higher performance
• Compiled a list of such contributions through the MVAPICH Website
  – [http://mvapich.cse.ohio-state.edu/best_practices/](http://mvapich.cse.ohio-state.edu/best_practices/)
• Initial list of applications
  – Amber
  – HoomdBlue
  – HPCG
  – Lulesh
  – MILC
  – MiniAMR
  – Neuron
  – SMG2000
• Soliciting additional contributions, send your results to mvapich-help at cse.ohio-state.edu. We will link these results with credits to you.
Amber: Impact of Tuning Eager Threshold

- Tuning the Eager threshold has a significant impact on application performance by avoiding the synchronization of rendezvous protocol and thus yielding better communication computation overlap
- 19% improvement in overall execution time at 256 processes
- Library Version: MVAPICH2 2.2b
- MVAPICH Flags used
  - MV2_IBA_EAGER_THRESHOLD=131072
  - MV2_VBUF_TOTAL_SIZE=131072
- Input files used
  - Small: MDIN
  - Large: PMTOP

Data Submitted by: Dong Ju Choi @ UCSD
MiniAMR: Impact of Tuning Eager Threshold

- Tuning the Eager threshold has a significant impact on application performance by avoiding the synchronization of rendezvous protocol and thus yielding better communication computation overlap
- 8% percent reduction in total communication time
- Library Version: MVAPICH2 2.2b
- MVAPICH Flags used
  - MV2_IBA_EAGER_THRESHOLD=32768
  - MV2_VBUF_TOTAL_SIZE=32768

Data Submitted by Karen Tomko @ OSC and Dong Ju Choi @ UCSD
UD-based transport protocol selection benefits the SMG2000 application.

- 22% and 6% on 1,024 and 4,096 cores, respectively.

- Library Version: MVAPICH2 2.1
- MVAPICH Flags used
  - MV2_USE_ONLY_UD=1

- System Details
  - Stampede@ TACC
  - Sandybridge architecture with dual 8-cores nodes and ConnectX-3 FDR network
• UD-based transport protocol selection benefits the SMG2000 application
• 15% and 27% improvement is seen for 768 and 1,024 processes respectively
• Library Version: MVAPICH2 2.2b
• MVAPICH Flags used
  – `MV2_USE_ONLY_UD=1`
• Input File
  – `YuEtAl2012`
• System Details
  – Comet@SDSC
  – Haswell nodes with dual 12-cores socket per node and Mellanox FDR (56 Gbps) network.
Partial subscription nature of hybrid MPI+OpenMP programming requires a new level of collective tuning
- For PPN=2 (Processes Per Node), the tuned version of MPI_Reduce shows 51% improvement on 2,048 cores

24% improvement on 512 cores
- 8 OpenMP threads per MPI processes

Library Version: MVAPICH2 2.1

MVAPICH Flags used
- The tuning parameters for hybrid MPI+OpenMP programming models is on by default from MVAPICH2-2.1 onward

System Details
- Stampede@ TACC
- Sandybridge architecture with dual 8-cores nodes and ConnectX-3 FDR network

HPCG: Impact of Collective Tuning for MPI+OpenMP Programming Model

- 24% improvement

Data Submitted by Jerome Vienne and Carlos Rosales-Fernandez @ TACC
• Partial subscription nature of hybrid MPI+OpenMP programming requires a new level of collective tuning
  – For PPN=2 (Processes Per Node), the tuned version of MPI_Reduce shows 51% improvement on 2,048 cores

• 4% improvement on 512 cores
  – 8 OpenMP threads per MPI processes

• Library Version: MVAPICH2 2.1

• MVAPICH Flags used
  – The tuning parameters for hybrid MPI+OpenMP programming models is on by default from MVAPICH2-2.1 onward

• System Details
  – Stampede@ TACC
  – Sandybridge architecture with dual 8-cores nodes and ConnectX-3 FDR network

Data Submitted by Jerome Vienne and Carlos Rosales-Fernandez @ TACC
Non-contiguous data processing is very common on HPC applications. MVAPICH2 offers efficient designs for MPI Datatype support using novel hardware features such as UMR.

UMR-based protocol selection benefits the MILC application.
- 4% and 6% improvement in execution time at 512 and 640 processors, respectively

Library Version: MVAPICH2-X 2.2b

MVAPICH Flags used
- MV2_USE_UMR=1

System Details
- The experimental cluster consists of 32 Ivy Bridge Compute nodes interconnected by Mellanox FDR.
- The Intel Ivy Bridge processors consist of Xeon dual ten-core sockets operating at 2.80GHz with 32GB RAM and Mellanox OFED version 3.2-1.0.1.1.
Hoomd-Blue: Impact of GPUDirect RDMA Based Tuning

- HoomdBlue is a Molecular Dynamics simulation using a custom force field.
- GPUDirect specific features selection and tuning significantly benefit the HoomdBlue application. We observe a factor of 2X improvement on 32 GPU nodes, with both 64K and 256K particles
- Library Version: MVAPICH2-GDR 2.2b
- MVAPICH-GDR Flags used
  - MV2_USE_CUDA=1
  - MV2_USE_GPUDIRECT=1
  - MV2_GPUDIRECT_GDRCOPY=1
- System Details
  - Wilkes@Cambridge
  - 128 Ivybridge nodes, each node is a dual 6-cores socket with Mellanox FDR

Data Submitted by Khaled Hamidouche @ OSU
Concluding Remarks

• Provided an overview of the different MVAPICH2 software libraries

• Presented details on configuration and runtime parameters, optimizations and their impacts for MVAPICH2 and MVAPICH2-GDR libraries

• Demonstrated best practices for several commonly used applications
MVAPICH2 – Plans for Exascale

- Performance and Memory scalability toward 1M cores
- Hybrid programming (MPI + OpenSHMEM, MPI + UPC, MPI + UPC++, MPI + CAF ...)
  - Support for task-based parallelism (UPC++)
- Enhanced Optimization for GPU Support and Accelerators
- Taking advantage of advanced features
  - User Mode Memory Registration (UMR)
  - On-demand Paging (ODP)
- Enhanced Inter-node and Intra-node communication schemes for upcoming OmniPath and Knights Landing architectures
- Extended RMA support (as in MPI 3.0)
- Extended topology-aware collectives
- Energy-aware point-to-point (one-sided and two-sided) and collectives
- Extended Support for MPI Tools Interface (as in MPI 3.0)
- Extended Checkpoint-Restart and migration support with SCR
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- M. Li (Ph.D.)

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- J. Zhang (Ph.D.)

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- R. Noronha (Ph.D.)
- X. Ouyang (Ph.D.)
- S. Pai (M.S.)
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Past Programmers
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Thank You!

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